P2L2 GmbH

SPI Sub IP Core Data Sheet

Key Features

- Configurable SPI clock phase and polarity
- Advanced synchronization scheme enables SPI clock frequency up to 1.66×system clock frequency: SPI clock rate can be higher than FPGA system clock rate
- Streaming interfaces to logic
- Optional CRC16 or CRC32 calculation
- Automated SPI frame/packed enumeration
- Fully synthesizable design
- Supports Intel/Altera Avalon and AXI streaming interfaces

Applications

- Resource efficient connection of FPGA to a microcontroller or SoC
- Allows even for low cost FPGA at high SPI data rates
- Coupling of FPGA to FPGA

Overview

Classical SPI Sub[1] IP cores require a very high FPGA system clock frequency $f_{\text{FPGA}} > 4 \times f_{\text{SPI}}$. Today even small, low-cost MCUs support $f_{\text{SPI}} >= 50\mathrm{M}Hz$ some go up to 100 MHz and higher. This results in a minimum f_{FPGA} of 200 MHz or 400 MHz respectively. Such frequencies are quite difficult, sometimes impossible to support with low-Power or low-cost FPGAs.

The advanced synchronization scheme of the P2L2 SPI Core is solving this problem by enabeling SPI clock frequency to be even higher than FPGA system frequency ($f_{\text{SPI}} > 1.66 \times f_{\text{FPGA}}$). This makes timing closure easily to be achieved for the FPGA system designer.

The SPI sub IP core can be used in an HDL description to establish communication with an SPI main (the common case is a microcontroller). The SPI Sub IP Core offers high flexibility to enable usage in a broad spectrume of applications. Fig. 1 shows a functional overview of the SPI sub IP core.

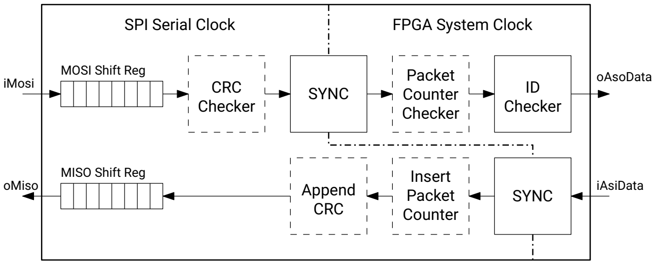

Figure 1: Functional overview of the SPI Sub IP Core.

MOSI

Serial data is received via the data line *iMosi*. A CRC16 or CRC32 can be calculated and checked directly on the serial SPI data as an option. In the event of an error, corresponding information is then be output on dedicated error lines.

Optionally, a consecutive packet number (byte modulo) can be checked as an additional means of error detection. This number is also useful for debugging purposes of the microcontroller software.

An SPI packet contains an ID (first or second byte, depending on whether the packet counter is activated) where every ID encodes a certain length of the SPI packet. This length is automatically checked for each SPI packet. The data is then made available for further

[1] The terms main and sub replace the traditionally used terms main and slave respectively in this document.

processing via a streaming interface (Avalon or AXI). This data of course is fully synchronous with the FPGA system clock used for the this interface.

MISO

In the opposite direction, data is sent back to the SPI main via the data line *oMiso*. The corresponding data has to be provided via a streaming interface (Avalon or AXI). This data is then synchronized into the serial SPI clock in the SPI sub IP core. A consecutive packet number can optionally be inserted as first byte of every packet which again serves for detection of missing packets. A CRC16 or CRC32 can also optionally be appended to the last bytes of the SPI packet.

Packet Protocol

The core translates SPI packets into parallel streaming data (AXI, Avalon) and vice versa considering that SPI itself is a streaming interface. The packet protocol can be freely choosen in the framing of a modulo packet number and ID at the start and error checking information on the end of the packet. Packet length per ID and invalid IDs are freely configurable by the user.

On customer demand P2L2 GmbH aids customers on finding their optimal packet protocol for a given application on the background of our vast experience gained from numerous projects.

Customer Options

The core comes already highly configurable, but can be additionally tailored to customer demands also, e.g.:

- Any type of CRC check or other error checking concepts
- Cryptification of packet data
- Customer choosen streaming interfaces on the FPGA side
- Memory mapped interface instead of streaming interface on FPGA side

Resource and Performance Measures

The advanced synchronization technique used by the core enables an outstanding SPI data rate in relation to FPGA system clock rate where data rate can even be higher than system clock rate. This feature especially lowers FPGA system clock rate demands when high SPI data rates are needed. At the same time the core is easy on timing closure and uses little resources in the FPGA.

Table 1 lists results for Efinix FPGAs by using the Efinity design environment version 2023.2.307. As the numbers show the SPI core will not be in the way for highest user design performance.

Table 1: Reachable SPI frequencies and resource results for maximum and minimum feature set of the core.

Family: Efinix Trion

FPGA	Feature Set	LUT	FF	f_{SPI}
T8F81C2	max	126	165	50 MHz
	min	68	100	54 MHz
T8Q144	max	126	165	128 MHz
	min	68	100	145 MHz
T120F576	max	126	165	124 MHz
	min	68	100	129 MHz

Family: Efinix Titanium

FPGA	Feature Set	LUT	FF	SPI Clk
Ti60F225	max	126	165	308 MHz
	min	68	100	354 MHz

Notes

1. The system frequency f_{FPGA} has to be at least $0.66 \times f_{\text{SPI}}$ or higher according to the needs of the customer design.
2. Timing constraints that the connected SPI Main (e.g. a microcontroller) demands may decrease maximum f_{SPI} from the values given in the table.
3. All results were reached with FPGAs of the C4 timing variant except the Trion T8F81 which is of the C2 timing variant.
4. Efinix FPGA families are based on the so called Quantum Fabric which uses XLR cells. These may be used as LUT cells or for routing purposes. The numbers of XLR cells used for routing purposes depends highly on the user design and are thus omitted from the table.